



## Chip Card & Security ICs

### SLE 5528

Intelligent 1024 Byte EEPROM  
with Write Protection and  
Programmable Security Code

<b>SLE 5528 Short Product Information</b>	
<b>Revision History: Current Version 2007-05-02</b>	
Previous Releases: 2006-11-24	
Page	Subjects (changes since last revision)
	Preliminary removed, editorial updates

**Important:** Further information is confidential and on request. Please contact:  
 Infineon Technologies AG in Munich, Germany,  
 Chip Card & Security ICs,  
 Fax +49 (0)89 / 234-955 9372  
 E-Mail: security.chipcard.ics@infineon.com

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**Warnings**

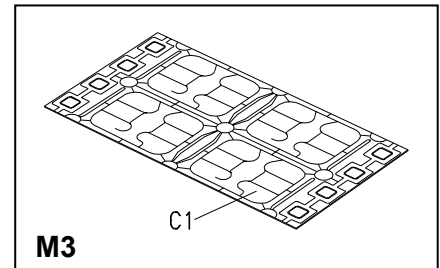
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## Intelligent 1024 Byte EEPROM with Write Protection and Programmable Security Code (PSC)

### Features

- **100% functional compatibility to SLE 4428**
- **1024 x 8 bit EEPROM organization of Data Memory**
- **1024 x 1 bit Protection Memory**
  - Byte-wise write protection of Data Memory (one time programmable)
  - Not alterable Manufacturer Code (chip coding and unique coding by application identifier RID according to ISO/IEC 7816-5)
- **Data Memory alterable only after verification of 2 Byte PSC**
- **PSC verification trials limited by Error Counter**
- **Serial synchronous three-wire link protocol according to ISO/IEC 7816**
  - Byte-wise addressing
  - End of processing indicated at data output
- **Contact configuration and Answer-to-Reset (synchronous transmission) in accordance to standard ISO/IEC 7816**
- **Electrical characteristics**
  - Ambient temperature range -40 ... +100°C for chip, -25 ... +80°C for module
  - Supply voltage 5V ± 10%
  - Supply current < 1 mA
  - EEPROM erase / write time 5 ms / 5 ms
  - ESD protection typically 4,000 V
  - EEPROM Endurance minimum 100,000 erase / write cycles<sup>1)</sup>
  - Data retention for minimum of 10 years<sup>1)</sup>
- **Advanced CMOS-technology optimized for security layout**
  - EEPROM-cells protected by shield
  - Shielding of deeper layers via metal
  - Sensory- and logical security functions
  - No insulation of backside necessary



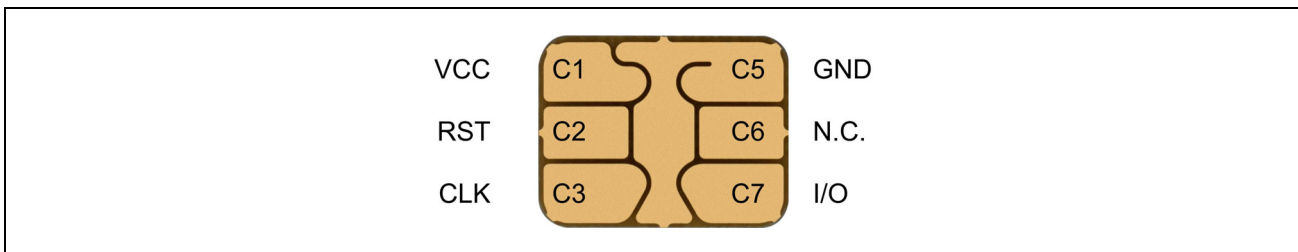
<sup>1)</sup> Values are temperature dependent.

## 1 Ordering and Packaging information

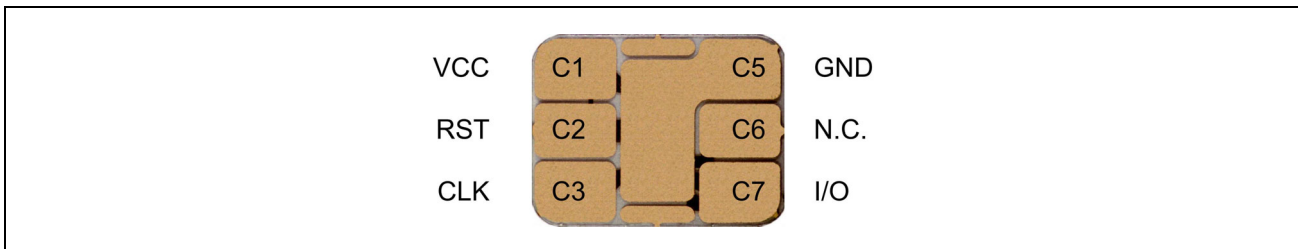
**Table 1 Ordering Information**

Type	Package <sup>1)</sup>	Remark	Ordering Code
SLE 5528 C	Die (on Wafer)	not sawn	on request
SLE 5528 D	Die (on Wafer)	Sawn	on request
SLE 5528 M3	T-M3.2-6		on request
SLE 5528 MFC3	S-MFC3.1-6-1	FCoS™	on request

### Pin Description



**Figure 1 Pin Configuration Wire-bonded Module M3.2 (top view)**



**Figure 2 Pin Configuration Module Flip Chip MFC3.1 (top view)**

<sup>1)</sup> Available as a Module Flip Chip (MFC3), wire-bonded module (M2 and M3) for embedding in plastic cards or as a die on non-sawn (C) / sawn wafer (D) for customer packaging

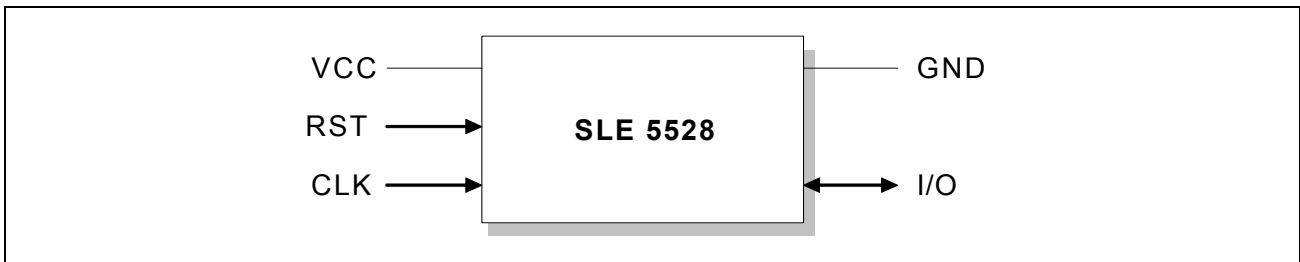


Figure 1 Pad Configuration Die

Table 2 Pin Definitions and Functions M3 / MFC3

Card Contact	Symbol	Function
C1	VCC	Supply voltage
C2	RST	Reset (Chip Enable)
C3	CLK	Clock input
C5	GND	Ground
C6	N.C.	Not connected
C7	I/O	Bi-directional data line (open drain)

## 2 Circuit Description

### Memory Organization

The memory is organized in a **Data Memory** of 1024 byte.

### Write Protection of Data Memory

**Write Protection Bits:** Each byte of the Data Memory can be irreversibly protected against data change by writing the corresponding bit in the **Write Protection Memory**. Dependent on the state of the protection bit the Data Memory is read only (ROM) or may be erased and written again (EEPROM). The manufacturer code (Application ID and Chip Coding) is programmed unalterable by the chip manufacturer.

### Programmable Security Code

Altering data in the Data Memory as well as setting a Write Protection Bit is only possible after verification of the 2-Byte **Programmable Security Code (PSC)**.

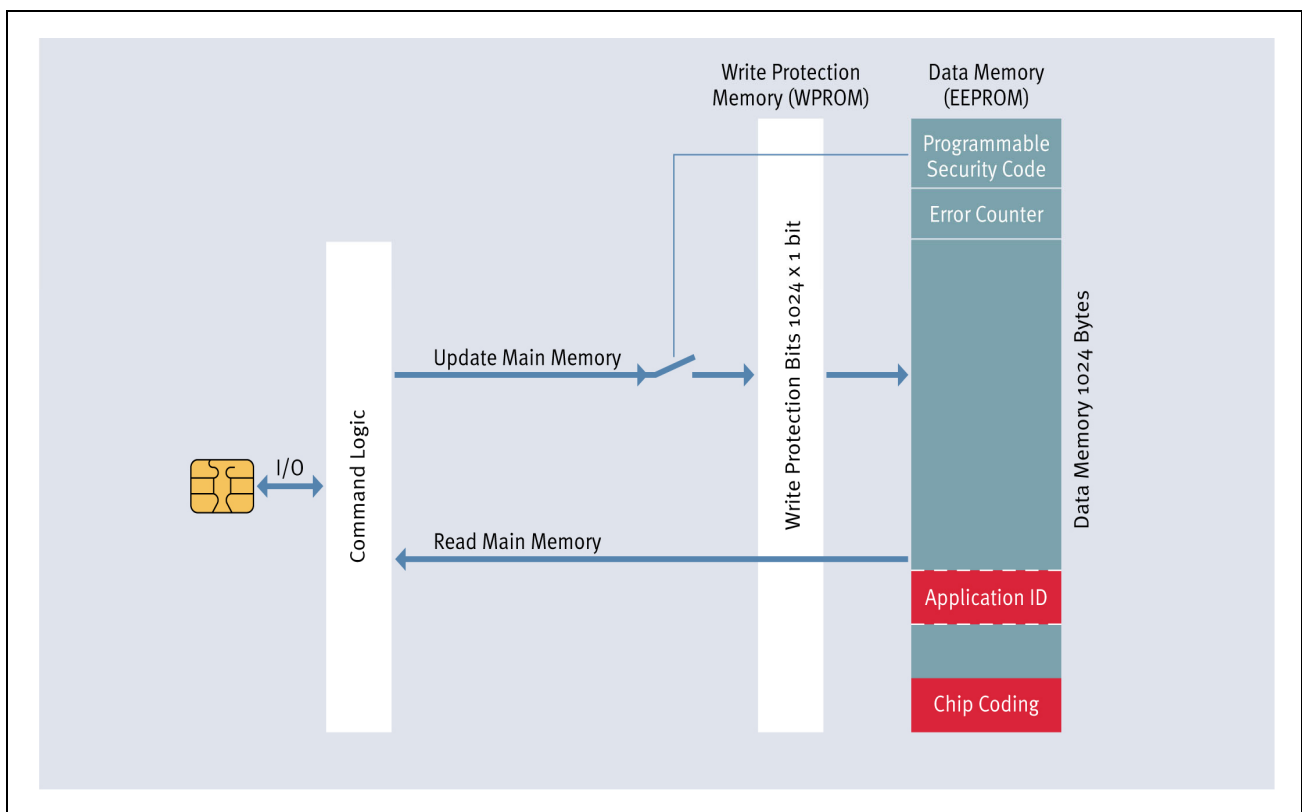


Figure 2 Memory Configuration SLE 5528